accordance with the generated drive waveform.

38. (NEW) A display apparatus including a display panel to display an image, comprising:

a clock generating circuit to generate a clock signal sequentially switched between a plurality of frequencies;

a drive waveform generating circuit generating a drive waveform having a frequency switched in accordance with said sequentially switched clock signal and driving the display panel in accordance with the generated drive waveform.

A8 cont.

39. (NEW) A display apparatus including a display panel to display an image, comprising:

a clock generating circuit; and

a drive waveform generating circuit generating a drive waveform by sequentially switching an output drive waveform between drive waveforms corresponding to a plurality of frequencies, and driving the display panel in accordance with the generated drive waveform.

REMARKS

STATUS OF CLAIMS

Claims 1-26 are pending.

Claims 3, 7, 11, 16, 20 and 24 are objected to but are indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 2, 4-6, 8-10, 12-15, 17-19, 21-23, 25 and 26 are rejected.

By this Amendment, claims 1-3, 5-7, 9, 11, 13-16, 18-20, 22-23 and 26 are amended and claims 27-39 are added. Therefore, claims 1-39 are now presented for consideration.

No new matter is presented and approval and entry is respectfully requested.

ALLOWABLE SUBJECT MATTER

In the Office Action at page 5, item 7, claims 3, 7, 11, 16, 20 and 24 are indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 7, 11, 16, 20 and 24 have not been rewritten in independent form since it is submitted that the independent claims, from which claims 3, 7, 11, 16, 20 and 24 depend, patentably distinguish over the cited art and should be allowable.

DRAWING OBJECTION

In the Office Action at page 2, item 2, the drawings are objected to because Figs. 1-6 lacked the label "Prior Art".

Figures 1-3

Enclosed herewith is a separate Letter to the Examiner Requesting Approval of Changes to the Drawings (Figs. 1-3), which are now labeled --Prior Art--, as suggested by the Examiner.

Figures 4-6

Figs. 4-6 represent a methodology of the Inventors with regard to the background of the invention and Figs 4-6 are not admitted prior art, but instead, are an analysis of the prior art which leads to the invention recited in claims 1-39.

AMENDMENTS TO CLAIMS 1-26

Claims 1-26 are amended to improve form without affect to scope of the claims as defined in *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 USPQ2d 1705 (US SupCt 2002).

REJECTION OF CLAIMS 1-26 UNDER 35 U.S.C. §103(a)

In the Office Action at pages 2-4, item 4, claims 1-2, 6, 10, 14-15, 19 and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kuwajima et al. (U.S. Patent No.: 6,339,422).

In the Office Action at page 4, item 5, claims 4, 8, 12, 17, 21 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kuwajima et al. as applied to claims 1, 6, 10, 14, 19 and 23 respectively in item 4, and further in view of Admitted Prior Art (in Applicants' Disclosure, page 7, lines 1-8 and Fig. 1)

In the Office Action at pages 4-5, item 6, claims 5, 9, 13, 18, 22 and 26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kuwajima et al. as applied to claims 1, 6, 10, 14, 19 and 23 respectively in item 4, and further in view of Tanaka et al. (U.S. Patent No.:

6,130,420).

Applicants respectfully traverse these rejections.

Independent Claims 1, 6, 10, 14, 19, and 23

As recited in the independent claim 1, "a clock signal used to drive a display panel is continuously varied in a frequency of the clock signal" and, as recited in claim 14, "a drive waveform generating circuit generating a drive waveform by using a clock signal from said clock generating circuit having a continuously varying frequency ... said drive waveform generating circuit drives said display panel by outputting the drive waveform having a varying frequency in accordance with said frequency varying clock signal," so as to spread out frequencies of the noise that the display panel emits and, thereby, to reduce peak values of the noise.

Further, as recited in claim 6, "peak noise output of the display panel is reduced by sequentially switching a clock signal, used to drive a display panel, between at least two frequencies" and, as recited in claim 19, a drive waveform generating circuit generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; ... said drive waveform generating circuit drives said display panel by outputting the drive waveform having a switched frequency in accordance with said sequentially switched clock signal," so as to spread out frequencies of the noise that the display panel emits and, thereby, to reduce peak values of the noise.

Further, as recited in claim 10, "said display panel is driven by sequentially switching an output drive waveform between said drive waveforms corresponding to said at least two frequencies" and, as recited in claim 23, "a drive waveform generating circuit generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; ... said drive waveform generating circuit drives said display panel by sequentially switching an output drive waveform between drive waveforms corresponding to at least two frequencies," so as to spread out frequencies of the noise that the display panel emits and, thereby, to reduce peak values of the noise.

As above-described, the purpose (effect) of the invention is to reduce peak values of noise by spreading out frequencies of the noise emitted by the display panel, and this purpose (effect) of the invention is different from that of Kuwajima et al. and Tanaka et al. Further, the distinguishing features of each of the independent claims 1, 6, 10, 14, 19 and 23, which are

above-described, are also different from that of Kuwajima et al and Tanaka et al.

Further, Applicant notes that as recited in claim 6 "switching a clock signal ... between at least two frequencies" is further limited by the recitation in claim 6 that "peak noise output of the display panel is reduced." Thus, the recitation in claim 6, as now once amended, is not suggested or disclosed by the cited art. (See also new dependent claims 32 and 33 which include a similar recitation to that of claim 6).

Kuwajima et al.

The purposes (effects) of Kuwajima et al. are performing "both the binary display and the gray-scale display without increasing power consumption when performing the binary display" (see Kuwajima et al. at column 10, lines 1-3); "saving the power consumed by the frequency divider 30" (see Kuwajima et al. at column 10, lines 9-10); driving "the LCD device with the lowest possible frame frequency (70 Hz in the binary display mode, and 140 Hz in the 16-level gray-scale display mode) for each display mode without causing flicker" (see Kuwajima et al. at column 10, lines 15-18); and "facilitating the use of the apparatus" by switching "between the binary display mode and the16-level gray-scale display mode" "without manually adjusting the contrast each time the display mode is switched [therebetween]" (brackets added) (see Kuwajima et al. at column 10, lines 26-29). Thus, the purposes (effects) of Kuwajima et al. are different from that the purpose of the invention (i.e., to reduce peak values of noise by spreading out the frequencies of the noise emitted by the display panel).

Further, the Kuwajima et al. display control circuit includes "a clock generator for generating a first clock signal having a single frequency; a frequency divider for dividing the frequency of the first clock signal generated by the clock generator, thereby providing a second clock signal; a selection signal generation section for generating a selection signal upon which one of a binary display mode and a gray-scale display mode is selected; a selector for selecting one of the first clock signal and the second clock signal based on the selection signal; and a display circuit for performing one of the binary display mode and the gray-scale display mode using the selected clock signal." (See Kuwajima et al. at column 2, lines 54-65.)

It is submitted that Kuwajima et al. does not disclose or suggest the recitations "a clock signal used to drive a display panel is continuously varied in a frequency of the clock signal" (of claim 1); "a drive waveform generating circuit generating a drive waveform by using a clock signal from said clock generating circuit having a continuously varying frequency; ... said drive waveform generating circuit drives said display panel by outputting the drive waveform having a

varying frequency in accordance with said frequency varying clock signal (of claim 14); "peak noise output of the display panel is reduced by sequentially switching a clock signal, used to drive a display panel, between at least two frequencies" (of claim 6); "a drive waveform generating circuit [for] generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; ... said drive waveform generating circuit drives said display panel by outputting the drive waveform having a switched frequency in accordance with said sequentially switched clock signal" (of claim 19); "said display panel is driven by sequentially switching an output drive waveform between said drive waveforms corresponding to said at least two frequencies" (of claim 10); and "a drive waveform generating circuit generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; ... said drive waveform generating circuit drives said display panel by sequentially switching an output drive waveform between drive waveforms corresponding to at least two frequencies" (of claim 23).

This is because, for example, Kuwajima does not discuss a continuously varying clock signal (see claim 1 and 14); sequentially switching a clock signal between at least two frequencies to reduce peak noise output of the display panel (see claim 6), sequentially switching an output drive waveform between said drive waveforms corresponding to at least two frequencies (see claims 10 and 23); and outputting the drive waveform having a switched frequency in accordance with said sequentially switched clock signal (see claim 19).

In the Kuwajima et al. method, it is possible to not cause flicker in both display modes (i.e., the binary display mode and the 16-level gray-scale display mode) by driving an LCD device with the lowest possible frame frequency (70 Hz in the binary display mode, and 140 Hz in the 16-level gray-scale display mode). Nevertheless, in the Kuwajima et al. method, in each of the binary display mode and the 16-level gray-scale display made, frequencies of noise emitted by a display panel are not spread out and peak values of the noise are not reduced, as the frame frequency is fixed in each of the binary display mode and the 16-level gray-scale display mode.

In contrast to the Kuwajima et al. method, in the invention recited in claims 1, 6, 10, 14, 19 and 23, the display panel is driven as above-mentioned. Thus, in the same display mode, peak values of noise are reduced by spreading out the frequencies of the noise emitted by the display panel.

Applicants' Disclosure (Admitted Prior Art)

The admitted prior art in applicant disclosure does not cure the deficiency of Kuwajima et al. as the admitted prior art discloses only a fixed-frequency clock signal.

Tanaka et al.

Tanaka et al. does not cure the deficiency of Kuwajima et al. This is because Tanaka et al. discloses a similar timing circuit to the circuit of Kuwajima et al. (i.e., which produce a frequency or a divided frequency selected in accordance with an operating mode.) More particularly, a "timing generating circuit 20 [of Tanaka et al.] comprises a reference oscillator 22, a divider 23 and a selector 24... that generates diverse timing signals" (brackets added). (See Tanaka et al. at column 4, line 47-50.) "The divider 23 divides the reference pulses oscillated by the reference oscillator 22 by a factor of m (1/m where m is a natural number). The selector 24 permits changeover between two choices either the reference pulses as oscillated by the reference oscillator 22, or the divided pulse signal from the divider 23. The switching action is carried out in accordance with the operating mode in effect." (See Tanaka et al. at column 4, line 59 to column 5, line 1.)

The cited prior art either taken singularly or in a proper combination neither discloses nor suggests the above-mentioned recitations in independent claims 1, 6, 10, 14, 19 and 23.

Accordingly, it is submitted that claims 1, 6, 10, 14, 19 and 23 are allowable.

Claims 2-5, 7-9, 11-13, 15-18 and 20-23, which depend from claims 1, 6, 10, 14, 19 and 23, are submitted to be allowable from the same reason as their respective independent claims, as well as for the additional recitations therein.

NEW CLAIMS 27-39

New claims 27-39 are presented to afford a varying scope of protection.

Entry and consideration are respectfully requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is respectfully requested solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 3/4/03

By: Eric Berkowitz
Registration No. 44,030

700 Eleventh Street, NW, Suite 500
Washington, D.C. 20001
(202) 434-1500

CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on March 4 ,20 03

STAAS & HALSEY

By: Eric Berkowitz

Date: 3/4/03

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please REPLACE claims 1-3, 5-7, 9, 11, 13-16, 18-20, 22-23 and 26 and ADD new claims 27-39 in accordance with the following:

1. (ONCE AMENDED) A driving method for a display apparatus, wherein a clock signal used [for driving] to drive a display panel is continuously varied in a frequency of the clock signal, and said display panel is driven with said frequency varying clock signal.

2. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 1, wherein said clock signal used [for driving] to drive said display panel is a source clock signal of said display apparatus.

3. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 1, wherein said clock used [for driving] to drive said display panel continuously varies within a range of plus or minus 1 percent of a reference frequency.

4. (AS UNAMENDED) The driving method for a display apparatus as claimed in claim 1, wherein said display apparatus is a plasma display apparatus.

5. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 1, wherein a control of said clock signal used [for driving] to drive said display panel is performed during a quiescent period.

6. (ONCE AMENDED) A driving method for a display apparatus having a display panel, wherein peak noise output of the display panel is reduced by sequentially switching [at least two frequencies are provided for] a clock signal, used to drive [for driving] a display panel, [by sequentially switching said clock] between [said] at least two frequencies[, said display panel is driven with said switched clock].

7. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 6, wherein two frequencies lying within plus or minus 1 percent of a reference frequency are set for said clock signal used [for driving] to drive said display panel.

8. (AS UNAMENDED) The driving method for a display apparatus as claimed in claim 6, wherein said display apparatus is a plasma display apparatus.

9. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 6, wherein a control of said clock signal used [for driving] to drive said display panel is performed during a quiescent period.

10. (AS UNAMENDED) A driving method for a display apparatus, wherein drive waveforms for a display panel are provided corresponding to at least two frequencies, and said display panel is driven by sequentially switching an output drive waveform between said drive waveforms corresponding to said at least two frequencies.

11. (AS UNAMENDED) The driving method for a display apparatus as claimed in claim 10, wherein said drive waveforms for said display panel are provided corresponding to two frequencies lying within plus or minus 1 percent of a reference frequency.

12. (AS UNAMENDED) The driving method for a display apparatus as claimed in claim 10, wherein said display apparatus is a plasma display apparatus.

13. (ONCE AMENDED) The driving method for a display apparatus as claimed in claim 10, wherein a control of said clock signal used [for driving] to drive said display panel is performed during a quiescent period.

14. (ONCE AMENDED) A display apparatus, comprising:

a clock generating circuit;[,]

a drive waveform generating circuit [for] generating a drive waveform by using a clock signal from said clock generating circuit having a continuously varying frequency; [from said clock generating circuit,] and

a display panel [for] displaying an image in accordance with said drive waveform, wherein[:

said clock generating circuit generates a clock whose frequency varies continuously, and] said drive waveform generating circuit drives said display panel by outputting [a] the drive

waveform having a varying [whose] frequency [varies] in accordance with said frequency varying clock signal.

15. (ONCE AMENDED) The display apparatus as claimed in claim 14, wherein said clock generating circuit generates [the] a source clock signal of said display apparatus.

16. (ONCE AMENDED) The display apparatus as claimed in claim 14, wherein said [clock generating circuit generates a] clock signal whose frequency varies continuously is within a range of plus or minus 1 percent of a reference frequency.

17. (AS UNAMENDED) The display apparatus as claimed in claim 14, wherein said display apparatus is a plasma display apparatus.

18. (ONCE AMENDED) The display apparatus as claimed in claim 14, wherein during a quiescent period, said clock generating circuit performs a control of said clock signal used [for driving] to drive said display panel.

19. (ONCE AMENDED) A display apparatus, comprising:

a clock generating circuit;[,]

a drive waveform generating circuit [for] generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; [from said clock generating circuit,] and

a display panel [for] displaying an image in accordance with said drive waveform, wherein[:

said clock generating circuit generates a clock sequentially switched between at least two frequencies, and] said drive waveform generating circuit drives said display panel by outputting [a] the drive waveform having a [whose] switched frequency [switches] in accordance with said sequentially switched clock signal.

20. (ONCE AMENDED) The display apparatus as claimed in claim 19, wherein said [clock generating circuit generates a] clock signal sequentially switched between two frequencies [lying] is within plus or minus 1 percent of a reference frequency.

21. (AS UNAMENDED) The display apparatus as claimed in claim 19, wherein said display apparatus is a plasma display apparatus.

22. (ONCE AMENDED) The display apparatus as claimed in claim 19, wherein during a quiescent period, said clock generating circuit performs a control of said clock signal used [for driving] to drive said display panel.

23. (ONCE AMENDED) A display apparatus, comprising:

a clock generating circuit;[,]

a drive waveform generating circuit [for] generating a drive waveform by using a clock signal from said clock generating circuit having a sequentially switched frequency switched between at least two frequencies; [from said clock generating circuit,] and

a display panel [for] displaying an image in accordance with said drive waveform, wherein[:] said drive waveform generating circuit drives said display panel by sequentially switching an output drive waveform between drive waveforms corresponding to at least two frequencies.

24. (AS UNAMENDED) The display apparatus as claimed in claim 23, wherein said drive waveform generating circuit sequentially switches said output drive waveform between drive waveforms corresponding to two frequencies lying within plus or minus 1 percent of a reference frequency.

25. (AS UNAMENDED) The display apparatus as claimed in claim 23, wherein said display apparatus is a plasma display apparatus.

26. (ONCE AMENDED) The display apparatus as claimed in claim 23, wherein during a quiescent period, said clock generating circuit performs a control of said clock signal used [for driving] to drive said display panel.

29. (NEW) A driving method for a display apparatus, comprising:

continuously varying a frequency of a clock signal; and

driving a display panel with said continuously varying frequency clock signal.

30. (NEW) The driving method for a display apparatus as claimed in claim 27, further comprising:

using the continuously varying frequency clock signal as a source clock signal of said display apparatus.

29. (NEW) The driving method for a display apparatus as claimed in claim 27, wherein the continuous varying of the frequency of the clock signal is within a range of plus or minus 1 percent of a reference frequency.

30. (NEW) The driving method for a display apparatus as claimed in claim 27, wherein said display apparatus is a plasma display apparatus.

31. (NEW) The driving method for a display apparatus as claimed in claim 27, further comprising:

performing a control of said clock signal used to drive said display panel during a quiescent period.

32. (NEW) The driving method for a display apparatus as claimed in claim 27, wherein said driving of the display panel reduces peak values of noise emitted by the display panel.

33. (NEW) The driving method for a display apparatus as claimed in claim 27, wherein said driving of the display panel spreads out frequencies of noise emitted by the display panel.

34. (NEW) A driving method for a display apparatus, comprising:

sequentially switching a clock signal between at least two frequencies; and

driving a display panel by with said sequentially switched clock signal to reduce peak values of noise emitted by the display panel.

35. (NEW) A driving method for a display apparatus, comprising:

providing drive waveforms for a display panel corresponding to a plurality of frequencies;

sequentially switching an output drive waveform between said drive waveforms

corresponding to said plurality of frequencies; and

driving said display panel by said drive waveforms corresponding to said plurality of frequencies.

36. (NEW) A display apparatus including a display panel to display an image, comprising:

a clock generating circuit to generate a clock signal having a continuously varying frequency; and

a drive waveform generating circuit generating a drive waveform having a frequency varying in accordance with said frequency varying clock signal and driving the display panel in accordance with the generated drive waveform.

37. (NEW) A display apparatus including a display panel to display an image comprising:

a clock generating circuit to generate a clock signal based on a spread-type clock oscillator; and

a drive waveform generating circuit generating a drive waveform having a frequency varying in accordance with the generated clock signal and driving the display panel in accordance with the generated drive waveform.

38. (NEW) A display apparatus including a display panel to display an image, comprising:

a clock generating circuit to generate a clock signal sequentially switched between a plurality of frequencies;

a drive waveform generating circuit generating a drive waveform having a frequency switched in accordance with said sequentially switched clock signal and driving the display panel in accordance with the generated drive waveform.

39. (NEW) A display apparatus including a display panel to display an image, comprising:

a clock generating circuit; and

a drive waveform generating circuit generating a drive waveform by sequentially switching an output drive waveform between drive waveforms corresponding to a plurality of

frequencies, and driving the display panel in accordance with the generated drive waveform.